WE CLAIM:

1. An inductor current emulation circuit for a switched-mode power supply (SMPS), comprising:

a SMPS which includes an inductor having first and second terminals and provides an output current at an output terminal, said SMPS arranged such that the current (I_L) in said inductor goes to zero at least once per switching cycle under static operating conditions, ,

an RC integrator connected in parallel across said inductor, comprising:

a resistor having first and second terminals, said resistor's first terminal connected to said inductor's first terminal, and

a capacitor having first and second terminals, said capacitor's first terminal connected to said resistor's second terminal at a first node and its second terminal connected to said inductor's second terminal,

a zero reset switch (ZRS) connected in parallel across said capacitor, and

a control circuit coupled to said ZRS and arranged such that said ZRS is open when I_L is essentially non-zero and such that said ZRS is closed during a least a portion of each switching cycle when I_L is essentially zero such that said capacitor is substantially discharged, such that the voltage (V_C) across said capacitor emulates I_L.

2. The inductor current emulation circuit of claim 1, wherein said RC integrator and said control circuit are arranged such that I_L is given by:

$I_L = V_C*R*(C/L)$,

where R is the resistor of said resistor, C is the

capacitance of said capacitor and L is the inductance of said inductor.

3. The inductor current emulation circuit of claim 1, wherein said SMPS is a discontinuous-inductor-current SMPS and said control circuit is arranged to receive V_C and to close said ZRS and substantially discharge said capacitor during a portion of each switching cycle when V_C is essentially zero.

4. The inductor current emulation circuit of claim 3, wherein said SMPS includes first and second output switches connected together at a second node, said inductor's first terminal and said resistor's first terminal connected to said second node, said SMPS arranged to operate said first and second output switches to effect said switching cycles such that each cycle consists of:

closing said first output switch and opening said second output switch such that current is conducted to said inductor until V_C reaches a predetermined peak value,

opening said first output switch and closing said second output switch such that current is conducted from said inductor, and

opening both first and second output switches when V_C reaches zero.

5. The inductor current emulation circuit of claim 1, wherein said SMPS is a continuous-bipolar-inductor-current SMPS, said emulation circuit further comprising a sensor which detects when current I_L crosses zero, said control circuit arranged to close said ZRS and substantially discharge said capacitor when said sensor detects a zero-crossing.

6. The inductor current emulation circuit of claim

5, wherein said SMPS includes first and second output switches connected together at a second node, said inductor's first terminal and said resistor's first terminal connected to said second node, said SMPS arranged to operate said first and second output switches to effect said switching cycles such that each cycle consists of:

closing said first output switch and opening said second output switch such that current is conducted to said inductor until V_C reaches a predetermined peak value, and

opening said first output switch and closing said second output switch such that current is conducted from said inductor until V_C reaches a predetermined minimum value.

7. The inductor current emulation circuit of claim 5, wherein said control circuit is arranged to close said ZRS and substantially discharge said capacitor when said sensor detects a negative-going zero-crossing.

8. The inductor current emulation circuit of claim 5, wherein said control circuit is arranged to close said ZRS and substantially discharge said capacitor when said sensor detects a positive-going zero-crossing.

9. The inductor current emulation circuit of claim 5, wherein said control circuit is arranged to close said ZRS and substantially discharge said capacitor when said sensor detects a negative-going zero-crossing, and when said sensor detects a positive-going zero-crossing.

10. The inductor current emulation circuit of claim 1, wherein said SMPS is a continuous-bipolar-inductor-current SMPS which requires information about I_L when I_L is of a first polarity but not the opposite, second polarity, said emulation circuit further comprising a sensor which

detects when current I_L crosses zero and becomes said second polarity, said sensor arranged to trigger said control circuit to close said ZRS and substantially discharge said capacitor when I_L is of said second polarity.

11. The inductor current emulation circuit of claim 1, wherein said ZRS is a transistor.

12. The inductor current emulation circuit of claim 1, wherein said SMPS is configured as a buck-type converter.

13. The inductor current emulation circuit of claim 1, wherein said SMPS is configured as a boost-type converter.

14. The inductor current emulation circuit of claim 1, wherein said SMPS is configured as a buck-boost type converter.